Hall Ticket Number:

Code No. : 14347 O

VASAVI COLLEGE OF ENGINEERING *(AUTONOMOUS)*, HYDERABAD

Accredited by NAAC with A++ Grade

B.E. (E.E.E.) IV-Semester Backlog Examinations, July-2022

Digital Electronics

Time: **3 hours** Max. Marks: **60**

*Note: Answer all questions from **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

Q. No.	Stem of the question	M	L	CO	PO
1.	Draw the symbol and write the logic expression of the two input universal logic gates.	2	2	1	1
2.	Define fan in and fan out characteristics of logic families.	2	1	1	1
3.	Draw block diagram and write the truth table of half subtractor.	2	2	2	1
4.	State the necessity of the multiplexer.	2	2	2	1
5.	Give the excitation table of JK flip flop.	2	2	2	1
6.	Define modulus of counter and write down the number of flip flops required for MOD-7 counter.	2	1	2	1
7.	A 4-bit R/2R digital-to-analog (DAC) converter has a reference of 5 volts. What is the analog output for the input code 0101.	2	3	3	1
8.	Mention the function of an analog to digital converter.	2	2	3	1
9.	Discuss programmable logic devices.	2	2	4	1
10.	Compare Static RAM and Dynamic RAM.	2	2	4	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Convert the following : i) $(5C7)_{16} = (?)_{10}$ ii) $(2598)_{10} = (?)_{16}$ iii) $(10110)_2 = (?)_{10} = (?)_{16}$	4	3	1	1
b)	Describe the operation of TTL logic circuit working as NAND gate.	4	2	1	1
12. a)	Minimize the following expression using K-map. $f(A, B, C, D) = \Sigma m (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$.	3	3	2	1
b)	Design a combination circuit to convert binary to gray code.	5	4	2	1

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13. a)	Explain the working of Master-Slave JK Flip-Flop with Truth Table and Logic diagram.	4	1	2	1
b)	Explain the operation of 3 bit synchronous up counter with Truth Table and Logic diagram	4	1	2	1
14. a)	a) Describe the operation of a DAC. b) What is the advantage of R/2R ladder DACs over those that use binary weighted resistors?	4	2	3	1
b)	Explain the working principle of Successive approximation type ADC with the help of block diagram.	4	1	3	1
15. a)	Discuss on the concept of working and applications of semiconductor memories.	4	2	4	1
b)	Implement the following functions using PLAs $F_1(x,y,z)=\sum m\ (1,2,4,6)$ $F_2(x,y,z)=\sum m\ (0,1,6,$ $F3(x,y,z)=\sum m\ (2,6)$	4	3	4	1
16. a)	Realize the following logic operations using only NAND gates: AND, OR, NOT	4	4	1	1
b)	Design full adder using two half adders and give the truth table of full adder	4	4	2	1
17.	Answer any ***two*** of the following:				
a)	Describe the operation of 4 bit SISO, PIPO shift registers with the help of block diagram and timing diagram.	4	2	2	1
b)	Discuss the following of Digital to Analog converters. a) Full-scale error. b) Settling time c) Offset error and its effect on a DAC output	4	2	3	1
c)	Compare PLA and PAL and draw the block diagrams of both.	4	2	4	1

M : Marks; L: Bloom's Taxonomy Level; CO; Course Outcome; PO: Programme Outcome

i)	Blooms Taxonomy Level – 1	20%
ii)	Blooms Taxonomy Level – 2	42.5%
iii)	Blooms Taxonomy Level – 3 & 4	37.5%

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